Accelerating Atomistic Simulation on Many-core Computing Platform

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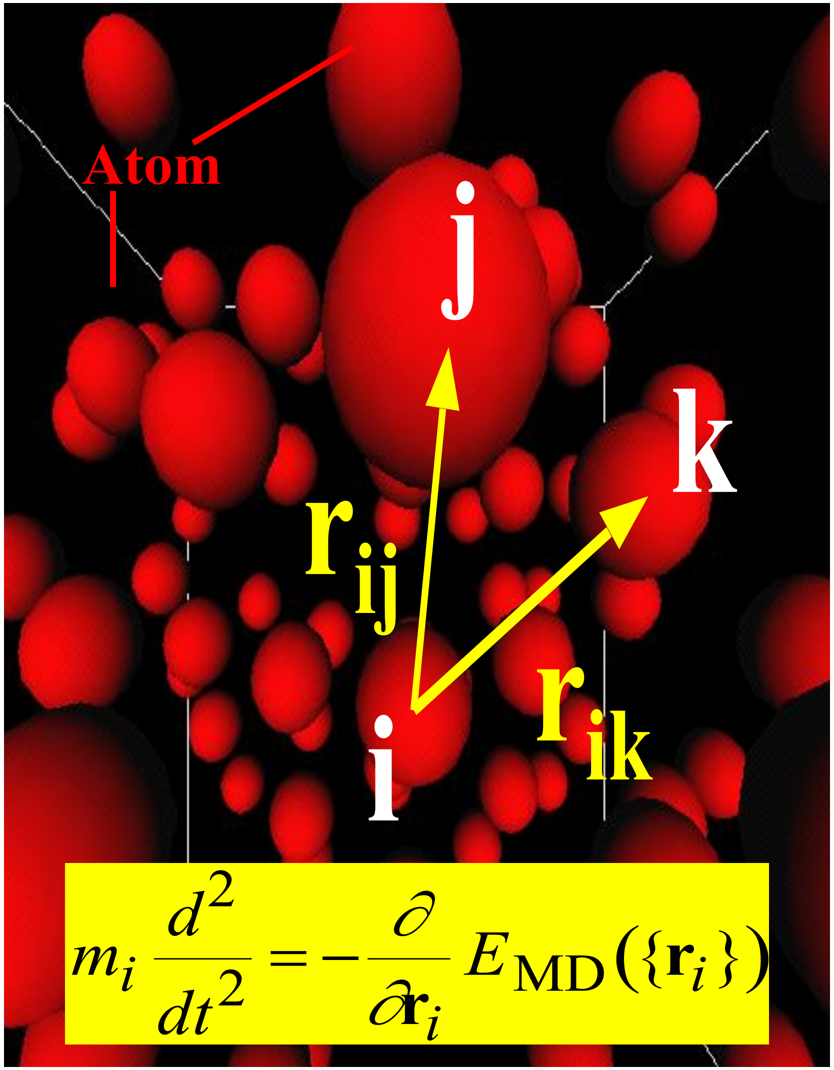
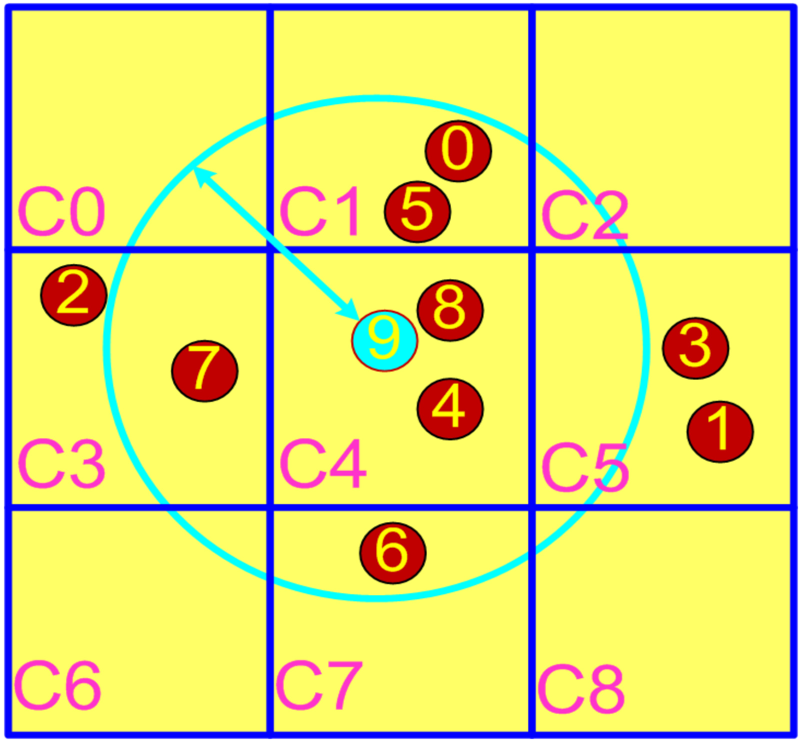
Atomistic Simulation

Molecular Dynamics (MD)



$$m_i \frac{d^2}{dt^2} = -\frac{\partial}{\partial \mathbf{r}_i} E_{\mathrm{MD}}(\{\mathbf{r}_i\})$$

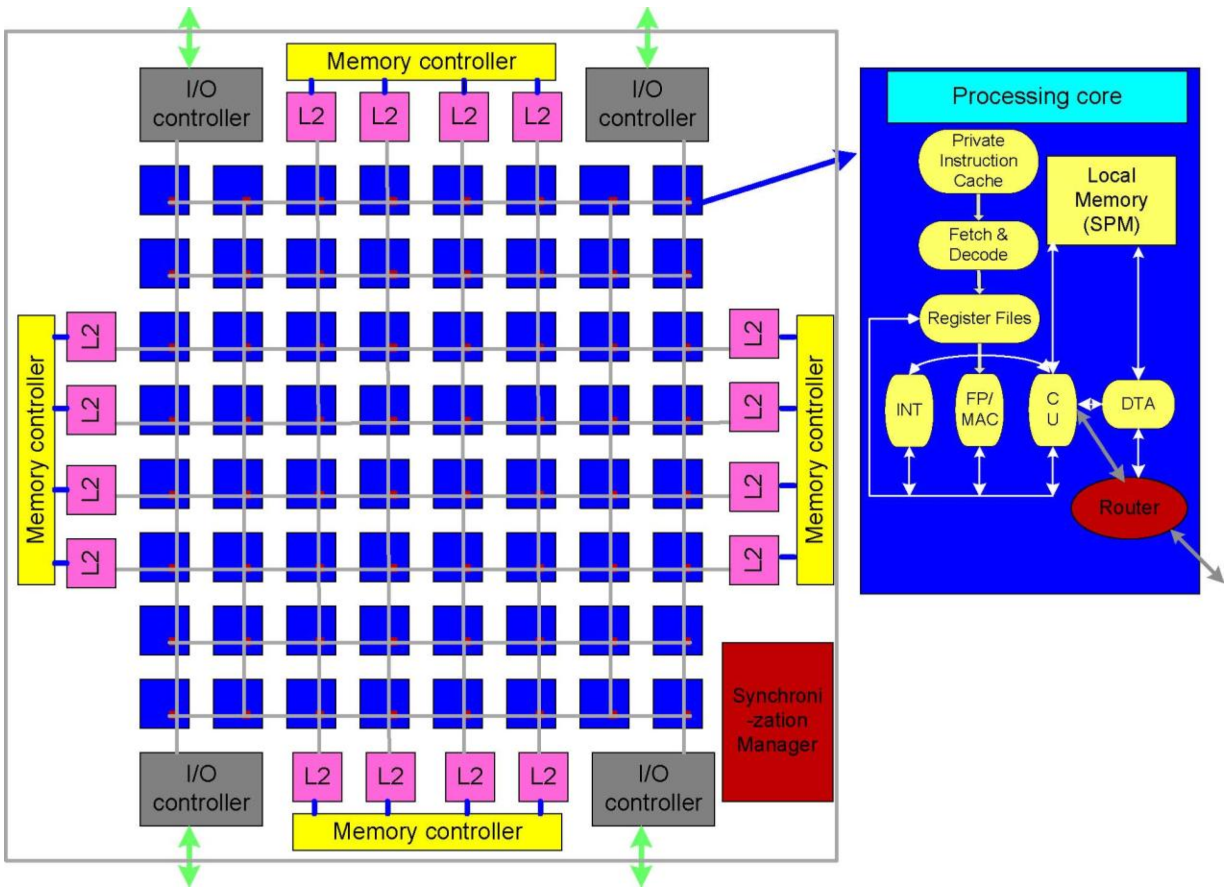
Linked-list cell method for MD



Irregular memory access
Frequent communication

GodsonT Many-core Computing Platform

64 core *GodsonT* many-core architecture



- **64 homogenous, dual-issue core 1GHz, 128Gflops in total**
- **lightweight hardware thread**
- **Explicit memory hierarchy**
- **16 shared L2 cache banks, 256KB each**
- **High bandwidth on-chip network: 2TB/s**

Optimization Strategy I
Adaptive Divide-and-Conquer(ADC)

- Purpose: estimate the upper bound of decomposition cell size where all data can fit into each core's local storage (SPM).
- Solution: recursively do cellular decomposition until the following Equation (adaptive to the size of each core's SPM) is satisfied.

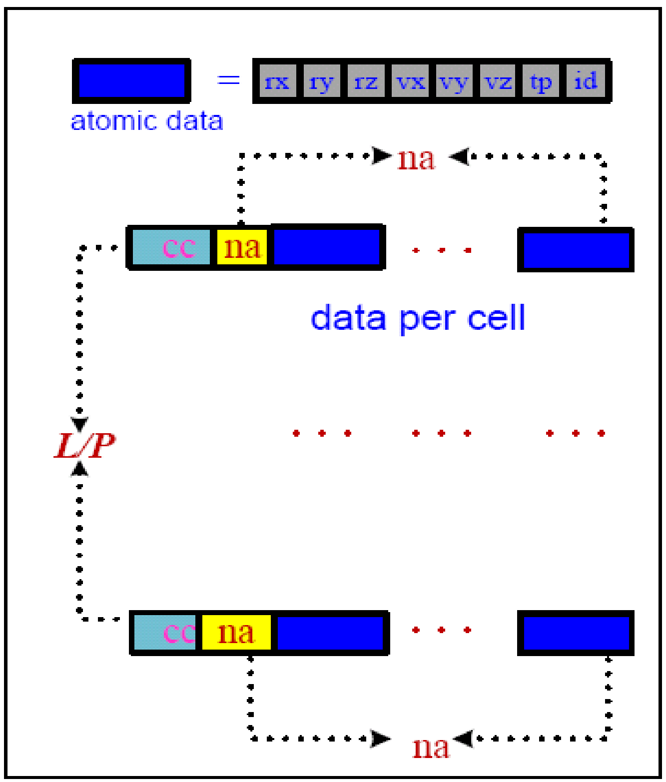
$$\left(\frac{L}{P}+N_b\right)\times qR_c^3\times B\le C_{pm}\Rightarrow R_c\le\sqrt[3]{\frac{PC_{pm}}{(PN_b+L)Bq}}$$

Estimation of the size of all data in a cell with cell size of *Rc*

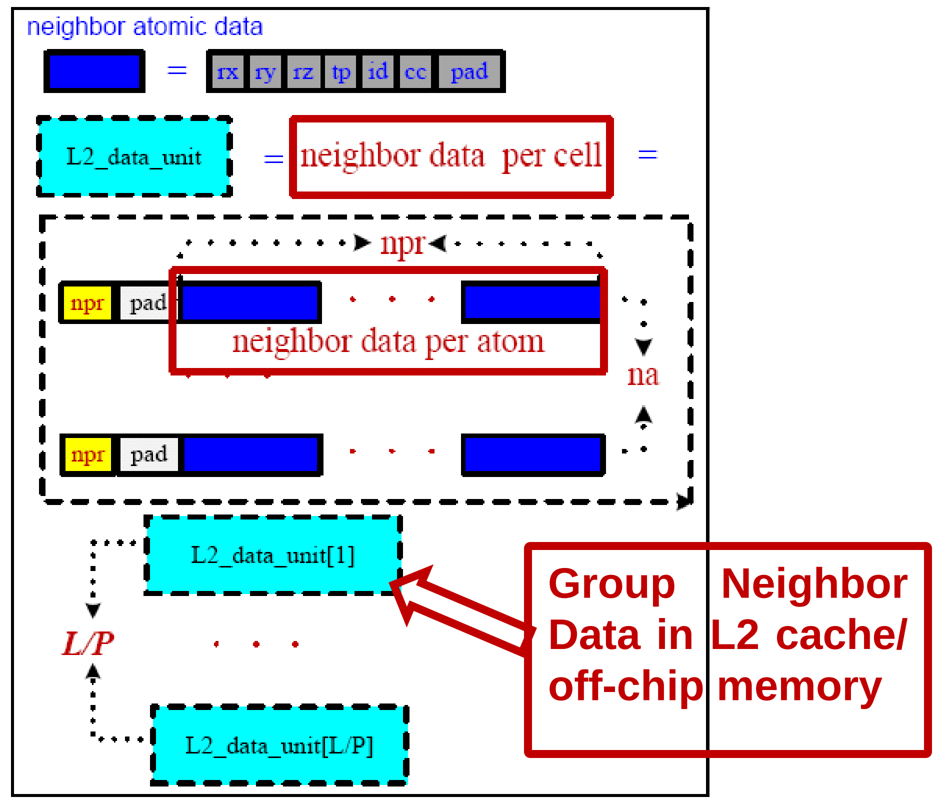
ADC + software controlled memory (decide when and where the data reside in SPM) to enhance the data usage.

Optimization Strategy II
Data Layout Optimization

- Purpose: ensure contiguous touching of data in each cell.
- Solution: data grouping/reordering + local-ID centered addressing.



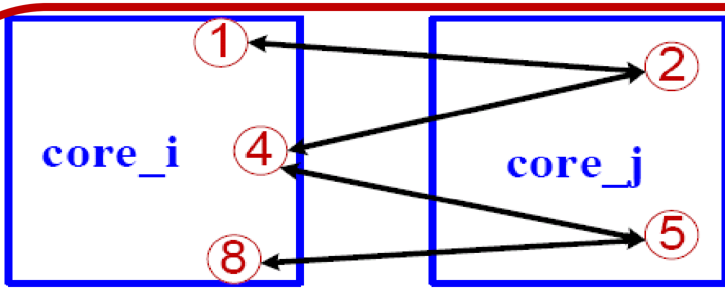
na: the number of atoms in one cell
cc: local-ID of each cell at one core



L2_data_unit is the data transfer unit from shared L2 cache or off-chip memory to LS via DMA-like operation

Optimization Strategy III
On-chip Locality Optimization

- Purpose: maximize data reuse for each cell.
- Solution: pre-processing to achieve locality-awareness, and further use locality-awareness to maximize data reuse.



parallel processing to achieve locality-awareness

core_i

PC[1]={2}
PC[4]={2, 5}
PC[8]={5}

core_j

PC[4]={2, 5}
PC[8]={5}

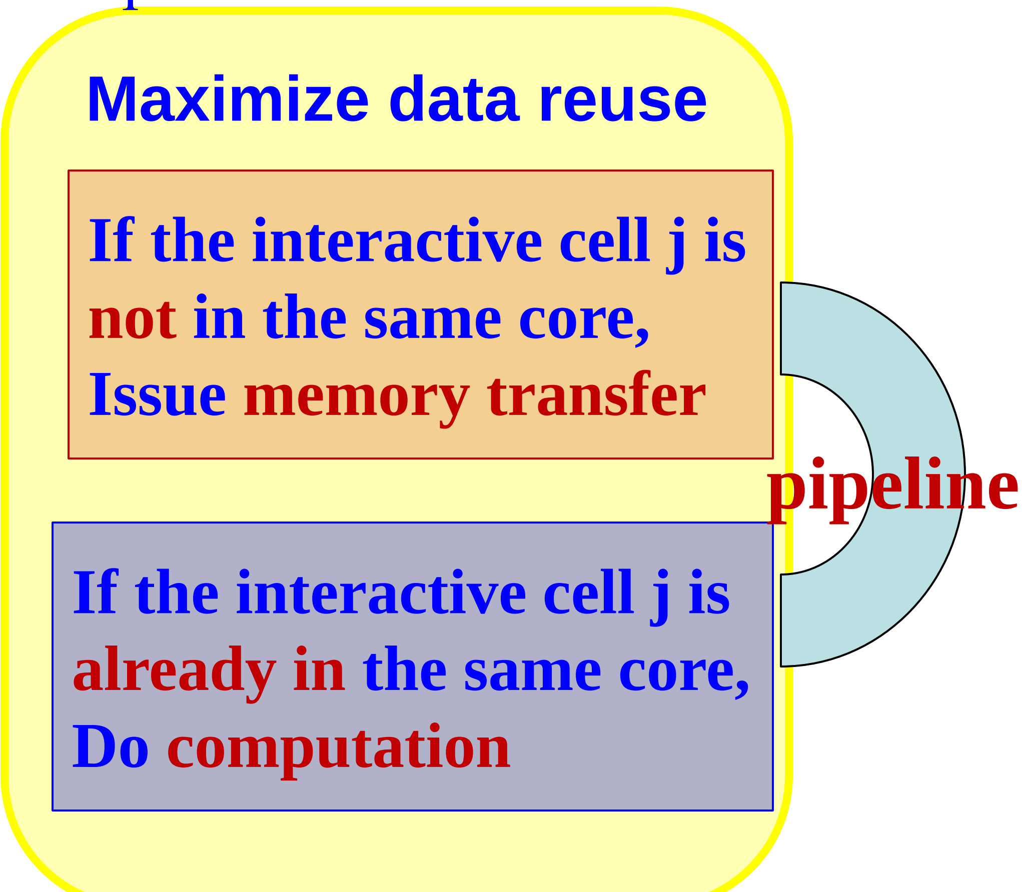
Maximize Data reuse

If cell_*k* in core_*i*,
Then
use *PC to* get all interactive cells
exhaust all the inter-computation.

architecture mechanism support for high-bandwidth core-core communication

Optimization Strategy IV Pipelining Algorithm

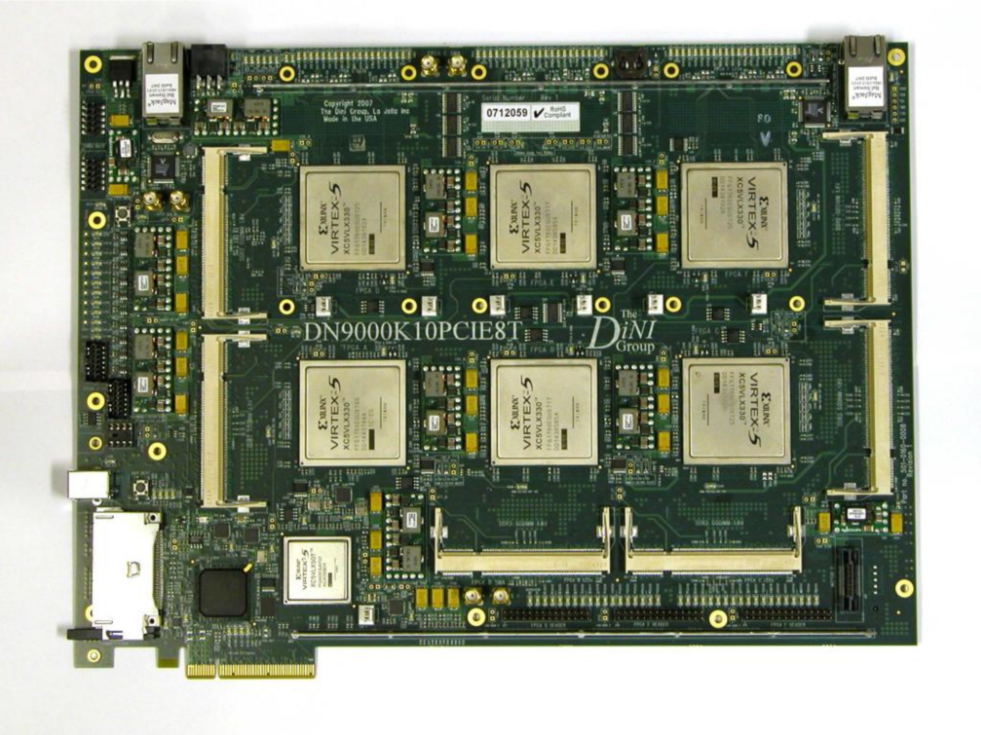
- Purpose: hide latency to access off-chip memory
- Solution: pipelining implemented via double buffered, asynchronized DTA operations.




```
tag_1 = tag_2 = 0
for each cell c_core_i [k] listed in PC[cj]
  if (tag_1 ≠ tag_2)
        DTA_ASYNC(spm_buf[1- tag_2],
              l2_dta_unit[c_core_i [k]])
      tag_2 = 1- tag_2
   endif
   calculate atomic interactions between
      c_core_i [k] and cj
    spm_buf[tag_1] ← cell c_core_i [k] 's
              neighbor atomic data
    tag_1= 1- tag_1
   endfor
   if (tag_1 ≠ tag_2)
        DTA_ASYNC(spm_buf[1- tag_2],
              l2_dta_unit[c_core_i [k]])
     tag_2 = 1- tag_2
   endif
```

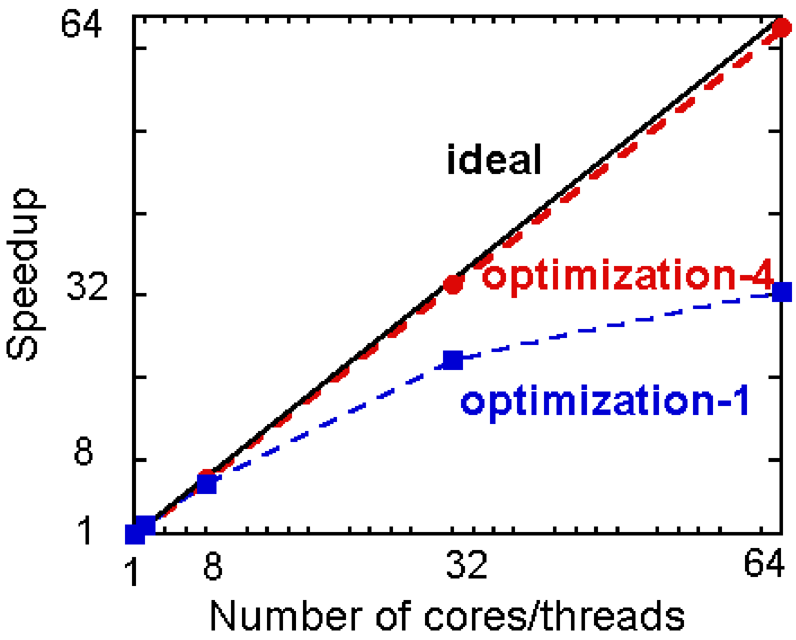
Performance Tests

FPGA emulator for 64 core *GodsonT*



On-chip strong scalability

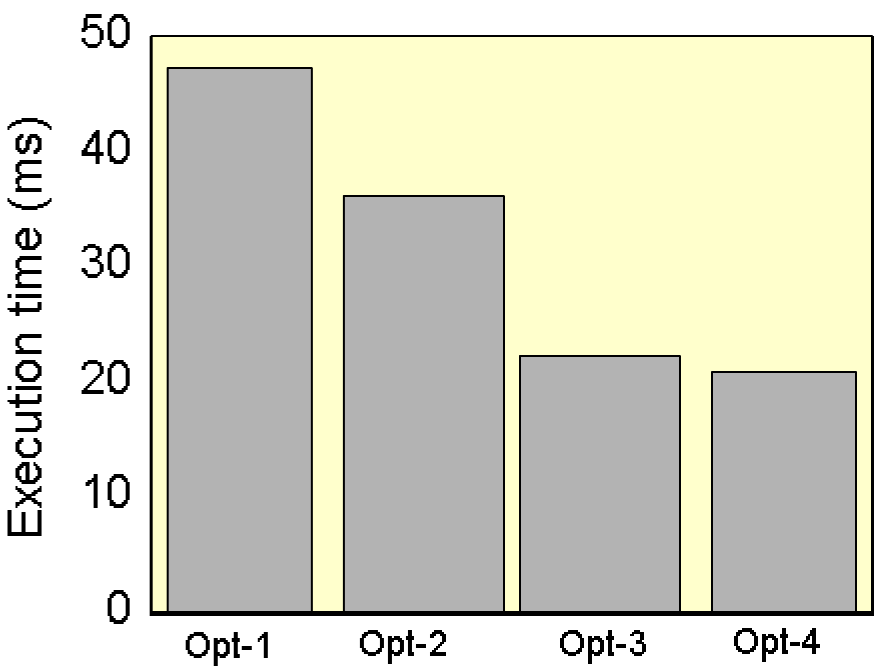
optimization-1:only ADC
optimization-4: all 4 optimizations



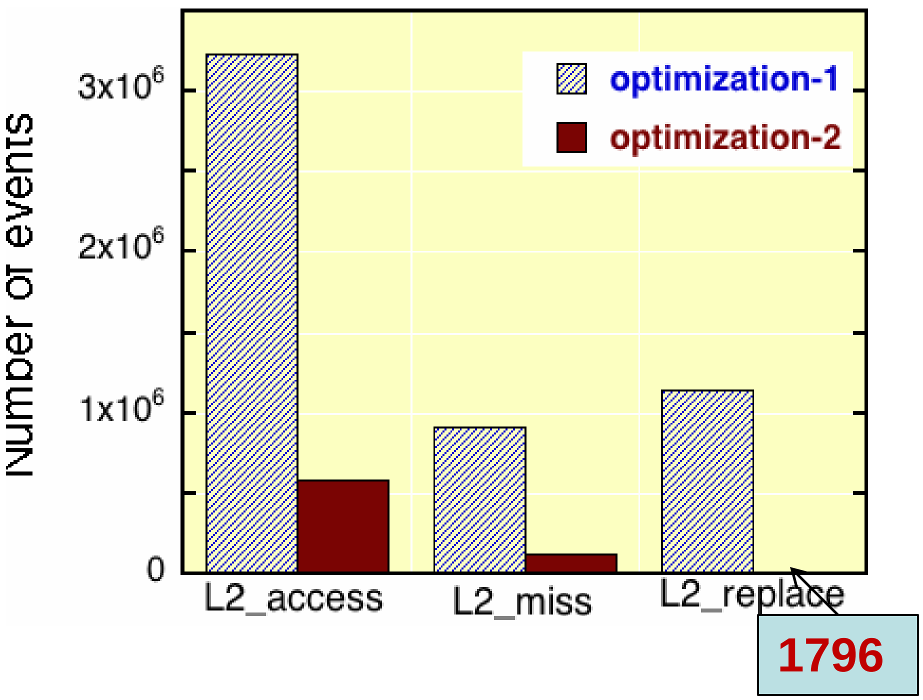
Excellent strong-scaling multithreading parallel efficiency of 0.99 on 64 cores with 24,000 atoms. (0.65 on 8-core multi-core)

Performance Analysis

Running time



L2 Cache performance

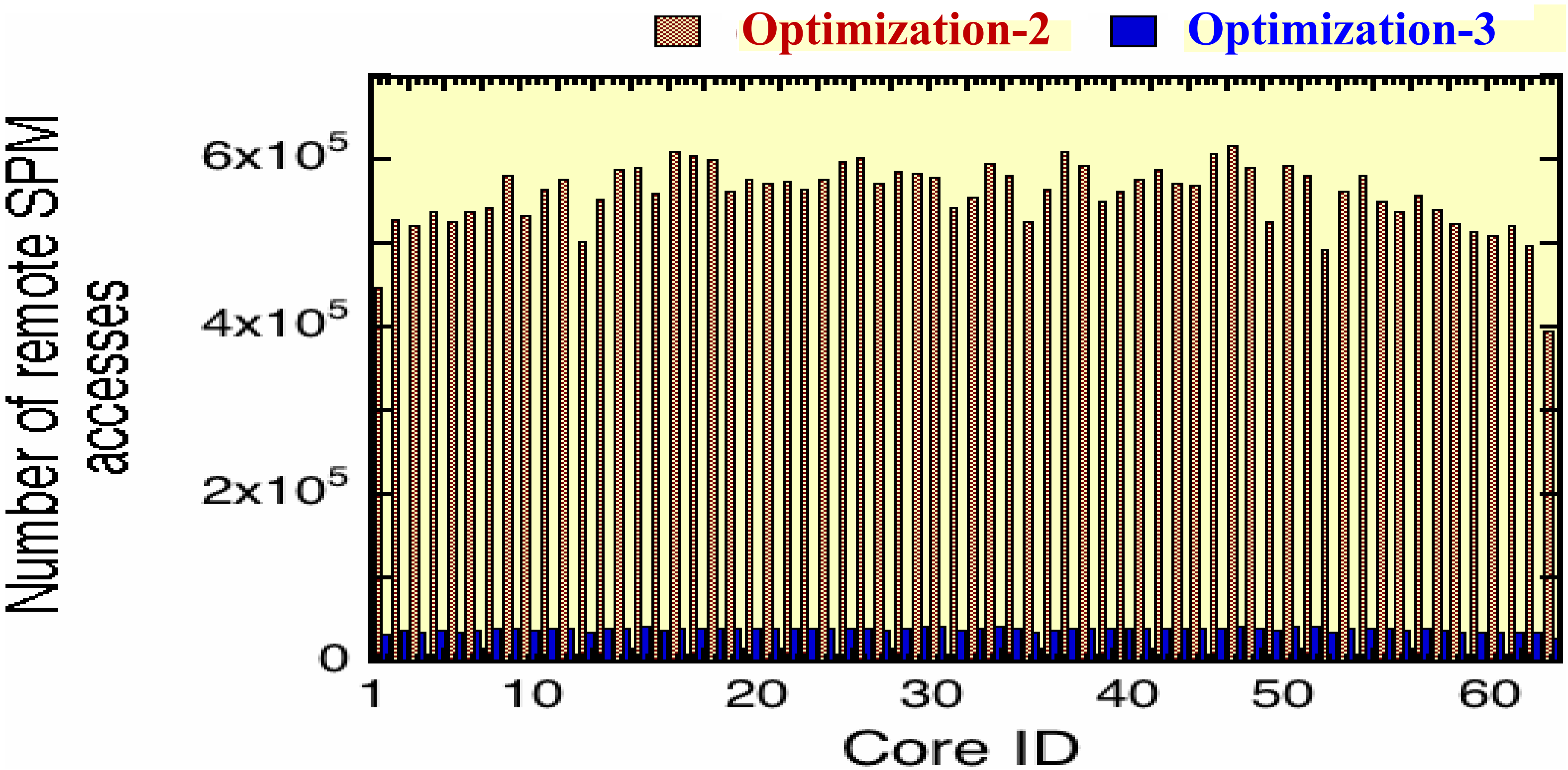


Running time is reduced two times.

All L2 cache events are reduced greatly.

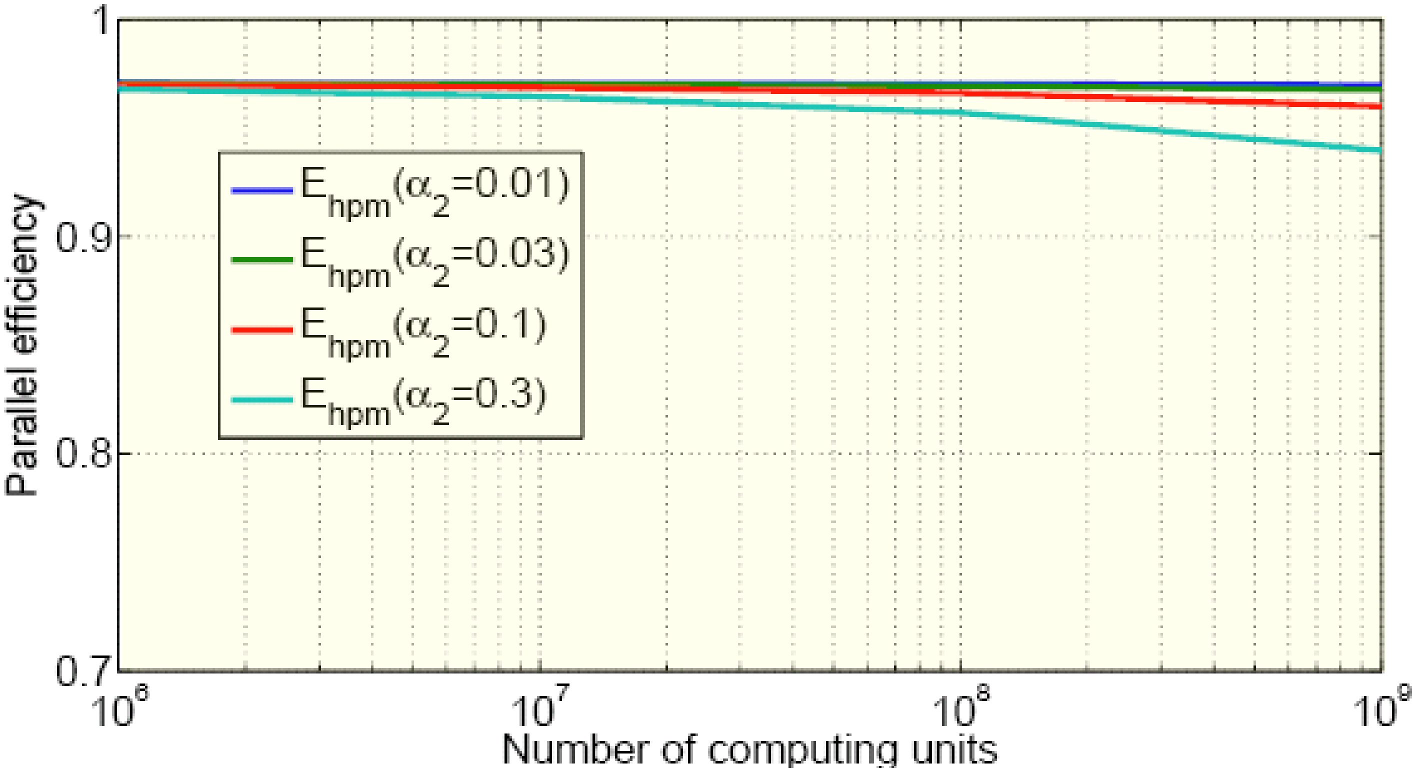
Performance Analysis

Remote memory access performance



Number of remote memory accesses is reduced to 7%.

Performance Model of Many-core Parallel System



Decent strong-scaling parallel efficiency over 0.9 up to billion processing elements with various core-core communication latency.

Conclusion

1. **Locality optimization utilizing architecture mechanism benefit strong scalability most.**

2. **Many-core architecture has the potential for future exascale parallel system.**

Thanks!

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